A 5.7-GHz 0.18-μm CMOS Gain-Controlled Differential LNA With Current Reuse for WLAN Receiver

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***Abstract*—This letter presents a 5.7 GHz 0.18 μm CMOS gain-controlled differential LNA for an IEEE 802.11a WLAN application. The differential LNA, fabricated with the 0.18 μm 1P6M standard CMOS process, uses a current-reuse technology to increase linear gain and save power consumption. The circuit measurement is performed using an FR-4 PCB test fixture. The LNA exhibits a noise figure of 3.7 dB, linear gain of 12.5 dB, $P_{1\,dB}$ of -11 dBm, and gain tuning range of 6.9 dB. The power consumption is 14.4 mW at $V_{DD} = 1.8$ V.**

***Index Terms*—0.18 μm, 5.7 GHz, CMOS, current reuse, differential LNA, WLAN.**

I. Introduction

DUE TO THE FAST growing demand for broadband wireless communications, the operating frequency is moving toward the 5 GHz U-NII band. The advantage of combining baseband and the RF front-end on one single chip for cost savings is strongly desired for highly integrated systems-on-chip (SOC) applications. Due to the speed improvements of the standard CMOS process, the unity gain frequency f_T of CMOS device becomes comparable to that in GaAs process. Recently, many RF circuits realized in the CMOS process have been reported and the 0.18 μm process is a good candidate for highly integrated SOC applications. The requirements of low power and low cost push the trend toward a single radio chip [1].

Two topologies of current-reused low noise amplifier have been reported. One topology is made of inductively degenerated NMOS and PMOS pairs in shunt configuration to achieve current reuse [2], [3]. The linearity is concerned due to the different mobility of NMOS and PMOS. The other topology is made of a two-stage common source amplifier to share the operating current and reduce current consumption [4], [5]. In this paper, a current-reuse topology of a two-stage common source amplifier is adopted to share the operating current [4]. The fully differential LNA topology can mitigate the effects of common mode noise and clock feedthrough. The function of controllable gain can prevents saturation of the receiver when the input signal is relatively large. The 5.7 GHz LNA is fabricated in a TSMC 0.18-μm standard CMOS process.

Manuscript received January 27, 2003; revised July 10, 2003. This work was supported by the National Science Council, Taiwan, R.O.C., under Grant NSC 91-2219-E-006-013. The review of this paper was arranged by Associate Editor Dr. Arvind Sharma.

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Digital Object Identifier 10.1109/LMWC.2003.819379

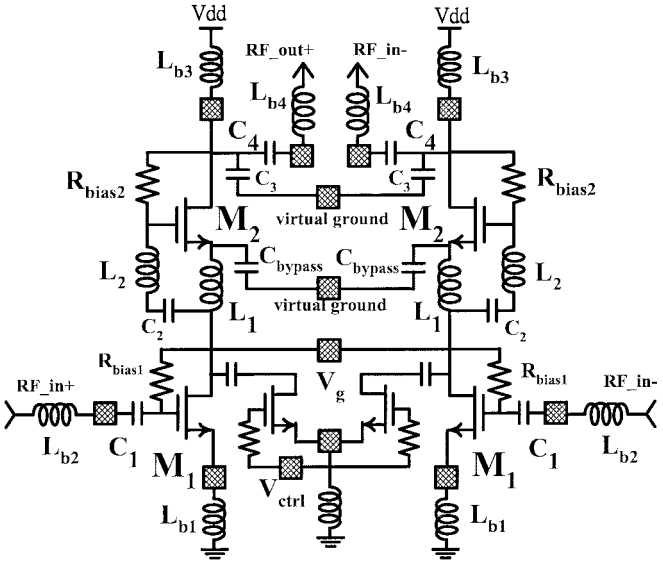

Fig. 1. Circuit schematic of a gain-controlled differential LNA with current reuse.

II. LNA Topology and Circuit Design

Fig. 1 illustrates the differential LNA with a current reuse topology. There are two virtual ground on the chip due to the chosen differential architecture. M_1 and M_2 transistors are both common source configurations, since the sources of M_1 and M_2 transistors are connected to signal ground separately. Two cascade common source amplifiers share the same supply current to reduce dc current consumption. Overall transconductance of the LNA topology is the multiplication of the transconductances of the two cascade amplifier. It provides gain expansion. V_g is a bias voltage of the first-stage common source amplifier. R_{bias1} and R_{bias2} are bias resistances. The bypass capacitance C_{bypass} achieves common source configuration of the second stage amplifier. L_{b1}–L_{b4} are bondwire equivalent inductances.

A. Input/Output and Inter-Stage Matching

From [6] the sources of noise and how to determine the gate width of the first stage transistor can be known. Under power consumption limit, the chosen gate width of the first stage transistor M_1 is $125(=25 \times 5)$ μm. Multi-finger layout technology is used to reduce noise source of the transistor gate resistance. To achieve input matching to the 50 Ω characteristic impedance of the system, we use series the bondwire equivalent inductance L_{b2}, the capacitance C_1 and the bondwire equivalent inductance

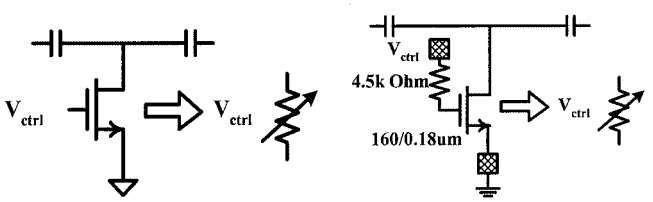

Fig. 2. Circuit schematic of gain-controlled switch transistor.

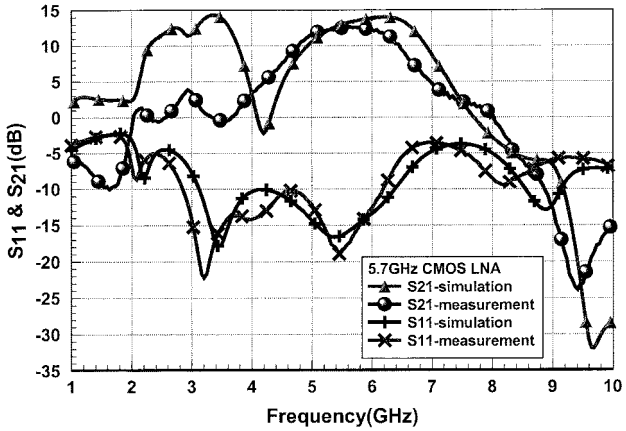

Fig. 3. Simulation and measurement results of the LNA gain and input return loss.

L_{b1} of source-degeneration. The bondwire equivalent inductance L_{b1} is used to match the real part of the input impedance to the characteristic impedance. The combination of gate and source bondwire equivalent inductance cancels the reactance of the parasitic capacitance C_{gs} at resonant frequency (ω_o) of the input transistor M_1. The expression of input impedance Z_{in} is shown as follows [6]:

$$Z_{\text{in}} = s(L_{b1} + L_{b2}) + \frac{1}{sC_{\text{gs}}} + \left(\frac{g_{m1}}{C_{\text{gs}}}\right) L_{b1}. \qquad (1)$$

When at resonant frequency $\omega_o(=1/\sqrt{(L_{b1}+L_{b2})C_{\text{gs}}})$

$$Z_{\text{in}} \approx \omega_T L_{b1} = 50\,\Omega \qquad (2)$$

where $\omega_T = g_{m1}/C_{\text{gs}}$.

The gate width of the second stage is chosen half of the first stage. Too large gate width is not stable for the circuit. On chip inductance L_1 is used for the first stage inductive load so the resonant frequency of the chosen on chip inductor L_1 is closed to operating frequency range. A choice of inductive load has another advantage which is no extra dc voltage drop. Series on chip inductance L_2 and capacitance C_2 perform conjugated matching between the first and second stage. Designing the parallel resonant frequency of bondwire equivalent inductance L_{b3} and capacitance C_3 close to operating frequency. Using series capacitance C_4 and bondwire equivalent inductance L_{b4} perform output matching to the characteristic impedance of the system.

B. Gain-Controlled Mechanism

Fig. 2 illustrates the gain-controlled mechanism. The voltage V_{ctrl} applied to the switched transistor, which needs no extra dc current consumption, controls the variable gain.

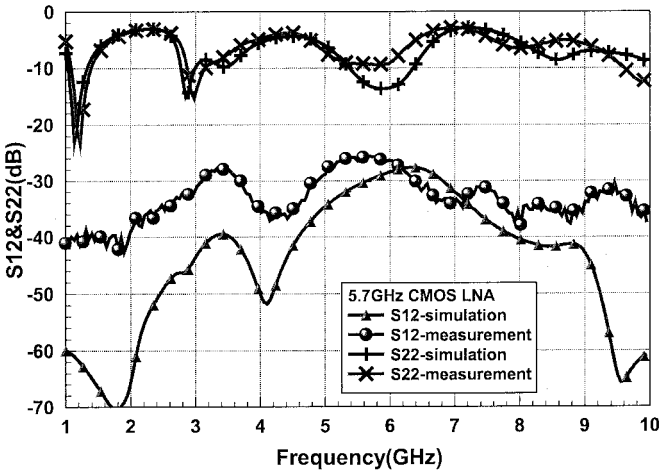

Fig. 4. Simulation and measurement results of the LNA S_{12} and S_{22}.

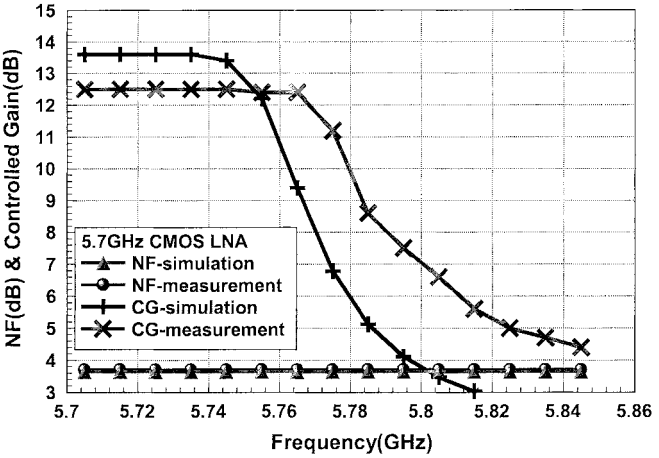

Fig. 5. Simulation and measurement results of the LNA noise figure and controlled gain range.

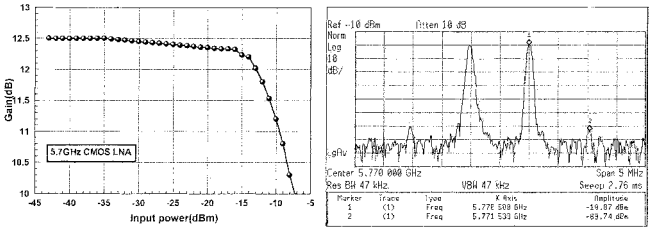

Fig. 6. Measured LNA gain compression and two tone test.

III. Simulation and Measured Results

The LNA measurements are performed on a FR-4 PCB test fixture. The LNA chip is connected to the test board with aluminum bond-wires. The effects of the bond-wires and the FR-4 test board are all taken into account in the simulations. The LNA gain and input return loss simulation and measurement results are shown in Fig. 3. Good agreement is achieved within the operating band 5.725–5.825 GHz. The measured gain is 12.5 dB and input return loss is 15 dB at 5.775 GHz. Fig. 4 shows the simulation and measurement results of S_{12} and S_{22}. Fig. 5 shows the simulation and measurement results of the noise figure and controllable gain range. The measured noise figure is 3.7 dB and controllable gain range is 3.6 to 12.5 dB (at $V_{\text{ctrl}} = 0$–1.8 V). The power consumption is 14.4 mW at $V_{\text{DD}} = 1.8$ V. Fig. 6

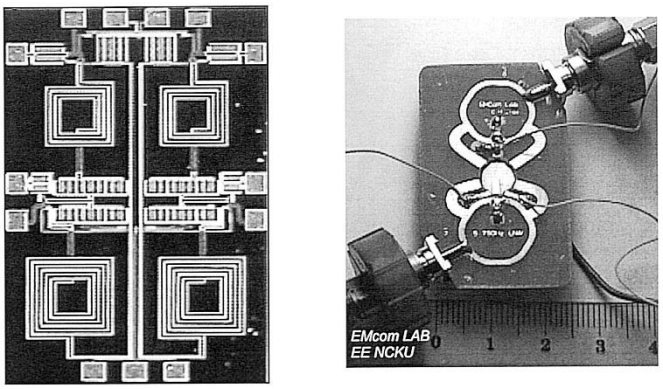

Fig. 7. Chip micrograph and photograph of the FR-4 PCB test board (with two 180° microstrip hybrid ring couplers) of the designed LNA.

TABLE I
SIMULATED AND MEASURED PERFORMANCE OF A 5.7 GHz 0.18-μm CMOS GAIN-CONTROLLED DIFFERENTIAL LNA

5.7GHz 0.18 m CMOS Gain-Controlled Differential LNA		
	Simulation	Measurement
DC	1.8V/8mA	1.8V/8mA
Input Return Loss	15.2dB	15dB
Output Return Loss	14dB	9dB
Gain	14.5dB	12.5
Controlled Gain@0~1.8V	14.5dB~3dB	12.5dB~3.6dB
Input P_{1dB}	-13.5dBm	-11dBm
IIP3	-3.3dBm	-0.45dBm
Noise Figure	3.65dB	3.7dB
Die size	0.958x1.455mm^2	

* The effect of the ring coupler has been taken into account in both simulation and measurement de-embedding.

shows the measured gain compression and two tone test. The input $P_{1\ dB}$ is -11 dBm and the input IP3 is -0.45 dBm. Fig. 7 shows the chip micrograph and photograph of the FR-4 PCB test board (with two 180° microstrip hybrid ring couplers) of the designed LNA. Note that there are two 5.7 GHz microstrip 180° hybrid ring couplers connected to the differential input and output ports of the LNA. This is to generate and combine a differential signal for measurement. The return loss of the ring coupler is higher than 20 dB and the insertion loss of that is about 1 dB at 5.7 GHz. The effect of the ring coupler has been taken into account in both simulation and measurement de-embedding. Table I summarizes the simulated and measured performance of the designed 5.7 GHz LNA.

IV. CONCLUSION

A 5.7 GHz CMOS gain-controlled differential LNA, fabricated in a TSMC 0.18 μm standard CMOS process, for an IEEE 802.11a WLAN application is presented. The LNA uses a current-reuse technology to increase linear gain and save power consumption. The measurements are performed using an FR-4 PCB test fixture. On the test fixture two 5.7 GHz microstrip 180° hybrid ring couplers are connected to the input and output ports of the LNA for differential measurement. The effect of the ring coupler has been taken into account in both simulation and measurement de-embedding. The LNA measurement at 5.775 GHz exhibits noise figure of 3.7 dB, linear gain of 12.5 dB, input/output return loss of 15 dB/9 dB, $P_{1\ dB}$ of -11 dBm, and gain tuning range of 3.6 to 12.5 dB with a power consumption of 14.4 mW at $V_{dd} = 1.8$ V. The low power consumption of the LNA suggests that the 0.18 μm CMOS process is useful for 5 GHz WLAN applications.

ACKNOWLEDGMENT

The authors would like to thank the Chip Implementation Center (CIC) of the National Science Council, Taiwan, R.O.C., for supporting the TSMC CMOS process.

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